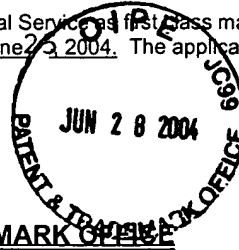


I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to : Commissioner of Patents and Trademarks, Alexandria, VA.22313, on June 25, 2004. The applicant and/or attorney requests the date of deposit as the filing date. Depositor: Karen Cinq-Mars

*Karen Cinq-Mars 6/25/04*  
(Signature & date)



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of \_\_\_\_\_: June 25, 2004  
An L Steegen et al. \_\_\_\_\_: Group Art Unit: 2812  
Serial No.10/605,906 \_\_\_\_\_: Examiner: Theresa Fredrick  
Filed: 11/05/2003 \_\_\_\_\_: International Business Machines Corporation  
2070 Route 52  
Hopewell Junction, NY 12533

**TITLE: Method and Structure For Forming Strained Si For CMOS Devices**

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

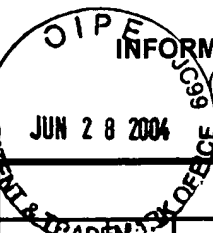
Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,  
An L. Steegen

By *Joseph P. Abate* 6-25-04  
Joseph P. Abate, Attorney  
Registration No. 30,238  
Telephone No. 845-894-4633

 <p><b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)</p>				ATTY DOCKET NO. <b>FIS920030236</b>		SERIAL NO. <b>10/605,906</b>	
				FILING DATE <b>11/5/03</b>		GROUP <b>2812</b>	
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,228,694	5/8/01	Doyle et al.			
		6,406,973	6/18/02	Lee			
		6,281,532	8/28/01	Doyle et al.			
		5,683,934	11/4/97	Candelaria			
		6,368,931	4/9/02	Kuhn et al.			
		5,330,446	5/10/94	Konishi et al.			
		4,853,076	8/1/89	Tsaur et al.			
		2002/0090791	7/11/02	Doyle et al.			
		2002/0074598	6/20/02	Doyle et al.			
		6,509,618	1/21/03	Jan et al.			
		6,476,462	11/05/02	Shimizu et al.			
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
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		6,362,082	3/26/02	Doyle et al.			
		6,228,694	5/8/01	Doyle et al.			
		5,565,697	10/15/96	Asakawa et al.			
		2003/0040158	2/27/03	Saitoh			
		2002/0086472	7/4/02	Roberds et al.			
		6,521,964	2/18/03	Jan et al.			
		6,506,652	1/14/03	Jan et al.			
		5,081,513	1/14/92	Jackson et al.			
		3,602,841	8/31/71	McGroddy			
		6,531,740	3/11/03	Bosco et al.			
		6,531,369	3/11/03	Ozkan et al.			

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	6,501,121	12/31/02	Yu et al.			
	6,498,358	12/24/02	Lach et al.			
	6,493,497	12/10/02	Ramdani et al.			
	6,403,975	6/11/02	Brunner et al.			
	6,361,885	3/26/02	Chou			
	6,255,169	7/3/01	Li et al.			
	6,246,095	6/12/01	Brady et al.			
	6,165,383	12/26/00	Chou			
	6,133,071	10/17/00	Nagai			
	6,046,464	4/4/00	Schetzina			
	6,025,280	2/15/00	Brady et al.			

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	5,940,736	8/17/99	Brady et al.			
	5,880,040	3/9/99	Sun et al.			
	5,861,651	1/19/99	Brasen et al.			
	5,679,965	10/21/97	Schetzina			
	5,670,798	9/23/97	Schetzina			
	5,561,302	10/1/96	Candelaria			
	5,471,948	12/5/95	Burroughes et al.			
	5,459,346	10/17/95	Asakawa et al.			
	5,391,510	2/21/95	Hsu et al.			
	5,371,399	12/6/94	Burroughes et al.			
	5,108,843	4/28/92	Ohtaka et al.			

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	5,060,030	10/22/91	Hoke			
	4,958,213	9/18/90	Eklund et al.			
	4,665,415	5/12/97	Esaki et al.			
	5,989,978	11/23/99	Peidous			
	6,284,626	9/4/01	Kim			
	6,274,444	8/14/01	Wang			
	6,261,964	7/17/01	Wu et al.			
	6,221,735	4/24/01	Manley et al.			
	6,117,722	9/12/00	Wuu et al.			
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					YES	NO		
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	6,066,545	5/23/00	Doshi et al.			
	6,008,126	12/28/99	Leedy			
	5,946,559	8/31/99	Leedy			
	5,840,593	11/24/98	Leedy			
	5,592,018	1/7/97	Leedy			
	5,592,007	1/7/97	Leedy			
	5,571,741	11/5/96	Leedy			
	5,557,122	9/17/96	Shirvastava et al.			
	5,354,695	10/11/94	Leedy			
	5,134,085	7/28/92	Gilgen et al.			
	5,006,913	4/9/91	Sugahara et al.			

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	4,952,524	8/28/90	Lee et al.			
	4,855,245	8/8/89	Neppl et al.			
	2002/0086497	7/4/02	Kwok			
	5,960,297	9/28/99	Saki			
	6,403,486	6/11/02	Lou			
	6,284,623	9/4/01	Zhang et al.			
	2003/0032261	2/13/03	Yeh et al.			
	2003/0057184	3/27/03	Yu et al.			
	6,265,317	7 / 24 / 01	Chiu et al.			
	2003/0067035	4/10/03	Tews et al.			
	6,461,936	10/8/02	von Ehrenwall			

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	6,319,794	11/20/01	Akatsu et al.			
	2001/0009784	7/26/01	Ma et al.			

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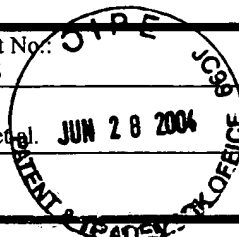
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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S  
INFORMATION DISCLOSURE STATEMENT

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Attorney Docket No.:  
FIS9-2003-0236Applicant:  
An L. Steegen, et al.Filing Date:  
11/5/03Serial No.:  
10/605,906Group:  
2812

## REFERENCE DESIGNATION

## U.S. PATENT DOCUMENTS

EXAMINERS INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

## FOREIGN PATENT DOCUMENTS

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						<input type="checkbox"/>	<input type="checkbox"/>

## OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

		Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998.
		Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99.
		Gregory Scott, et al., "NMOS Drive Current Reduction Caused by Transistor Layout and Trench Isolation Induced Stress", International Electron Devices Meeting, 34.4.1, IEEE, September 1999.
		F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000.
		Shinya Ito, et al., "Mechanical Stress Effect of Etch-Stop Nitride and its Impact on Deep Submicron Transistor Design", International Electron Devices Meeting, 10.7.1, IEEE, April 2000.
		A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001.
		K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002.

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